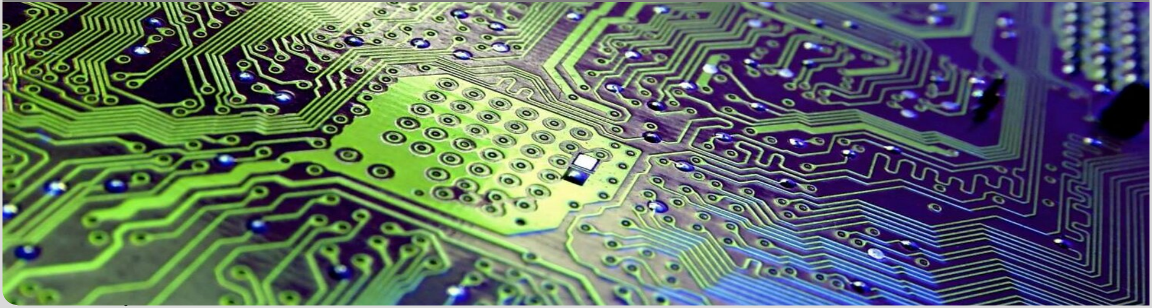
Karlsruher Institut für Technologie

FPGAhammer: Remote Voltage Fault Attacks on Shared FPGAs, suitable for DFA on AES

Jonas Krautter, Dennis R.E. Gnad, Mehdi B. Tahoori | 10.09.2018

INSTITUTE OF COMPUTER ENGINEERING – CHAIR OF DEPENDABLE NANO COMPUTING



Motivation

- More resources per FPGA ⇒ **Multi-user** environments:
  - Amazon, Microsoft and introduce FPGA usage in cloud computing
  - System-on-Chip (SoC) variants, tightly coupled FPGA based systems (Xilinx PYNQ, Intel Xeon FPGA, Intel/Altera-SoCs...)
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- New attack scenarios:
  - Passive on-chip side-channels[1]
  - Denial-of-Service[2]
  - **This work: Fault attacks**
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- Proof-of-Concept work: Successful DFA on AES

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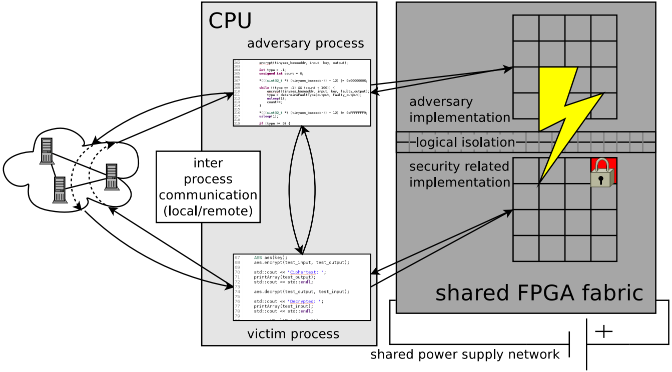
Threat model



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        encrypt(tinyaes_baseaddr, input, key, output);

        int type = -1;
        unsigned int count = 0;

        *(((uint32_t *) (tinyaes_baseaddr)) + 12) |= 0x00000006;

        while ((type == -1) && (count < 100)) {
            encrypt(tinyaes_baseaddr, input, key, faulty_output);
            type = determineFaultType(output, faulty_output);
            usleep(1);
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        if (type >= 0) {
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    std::cout << "Ciphertext: ";
    printArray(test_output);
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CPU
adversary process
inter process communication (local/remote)
victim process
adversary implementation
logical isolation
security related implementation
shared FPGA fabric
+
shared power supply network

- Shared FPGA fabric ⇒ **Shared Power Distribution Network (PDN)**

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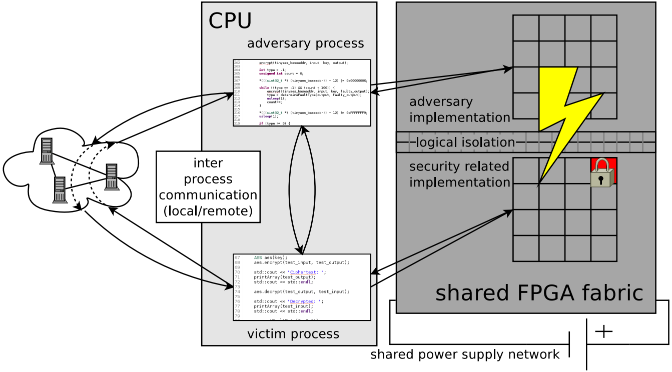
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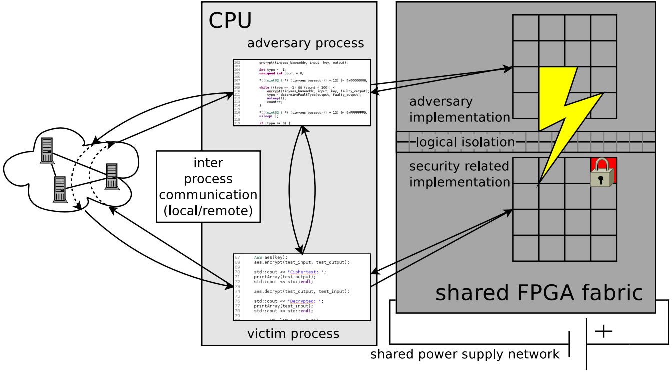
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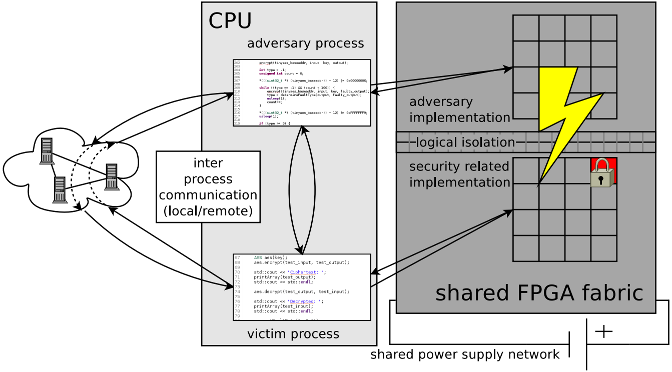
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- **Chosen-Plaintext Attack** scenario

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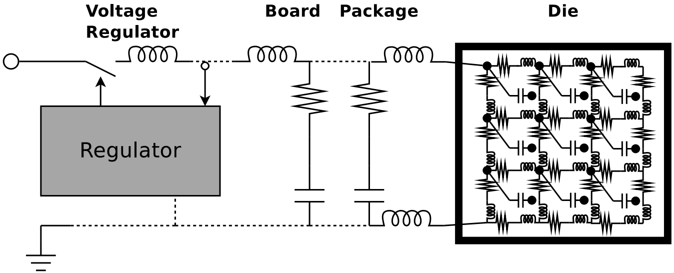
- Interconnections from the voltage regulator down to logic elements
- Model: RLC-mesh (Resistive, Inductive and Capacitive elements)



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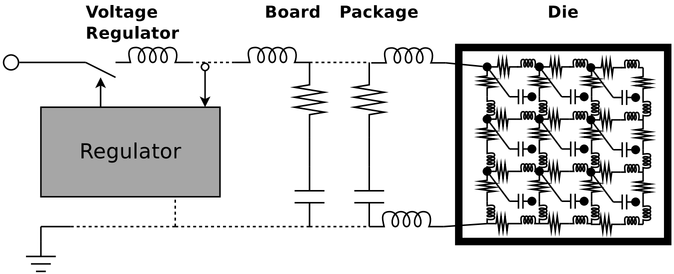

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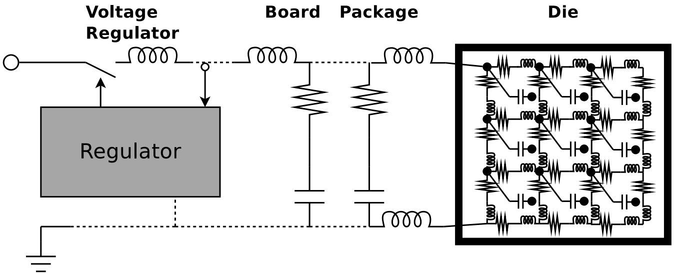

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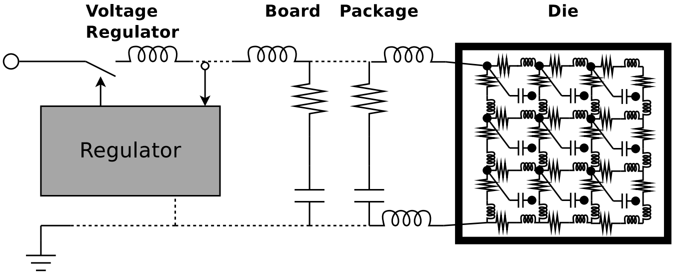
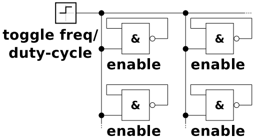


- Law of Inductance: $V_{\text{drop}} = I \cdot R + L \cdot \frac{dI}{dt}$
- High current variation ⇒ Power supply voltage variation
- Lower supply voltage ⇒ **Timing faults**

Malicious Logic



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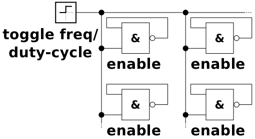

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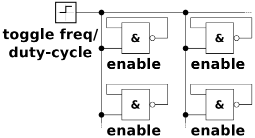

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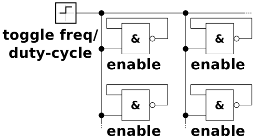

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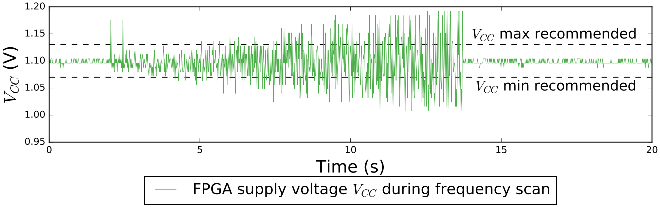

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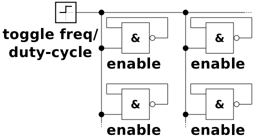

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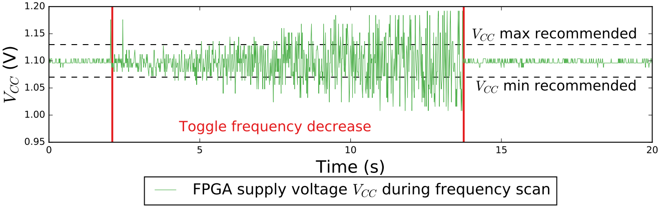

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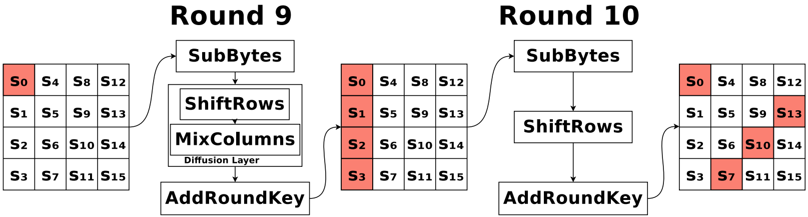

Round 9

🟥 S_0	S_4	S_8	S_{12}
S_1	S_5	S_9	S_{13}
S_2	S_6	S_{10}	S_{14}
S_3	S_7	S_{11}	S_{15}

SubBytes

ShiftRows

MixColumns

Diffusion Layer

AddRoundKey

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SubBytes

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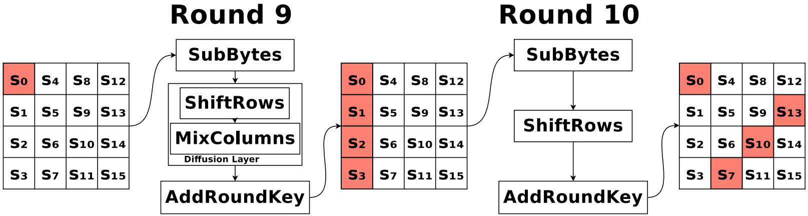

- Successful injection can be **verified**

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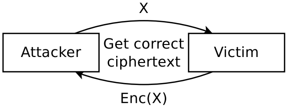
Fault Injection and Analysis

- Attacker issues encryption request to get correct ciphertext



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- Attacker issues encryption request to get correct ciphertext
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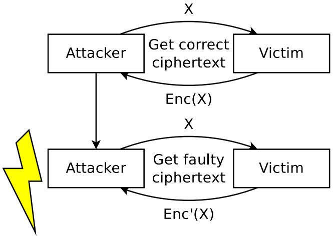

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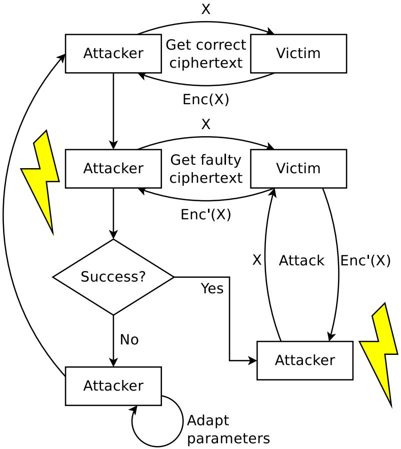

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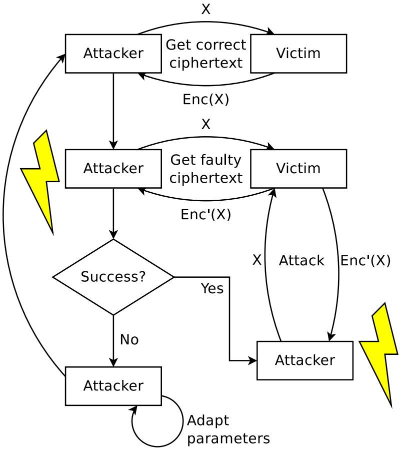
- Calibration is done only **once** for a specific board



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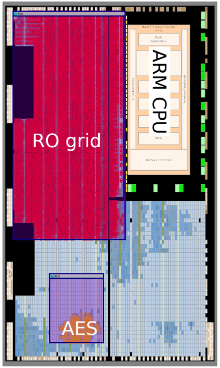

- FPGA boards: 3× Terasic DE1-SoC, 1× Terasic DE0-Nano-SoC
  - 3 boards of the same type
  - 2 different boards

    ⇒ Show generality of attack
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- Linux environment on ARM Cortex-A9

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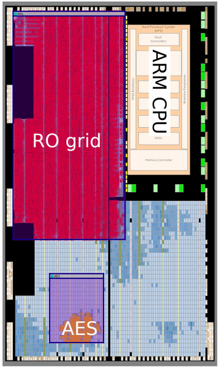

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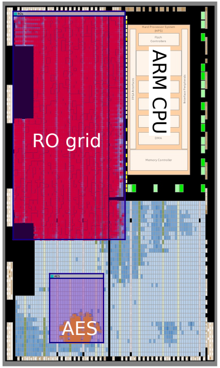

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- Fault injection on SoC, Key recovery on PC

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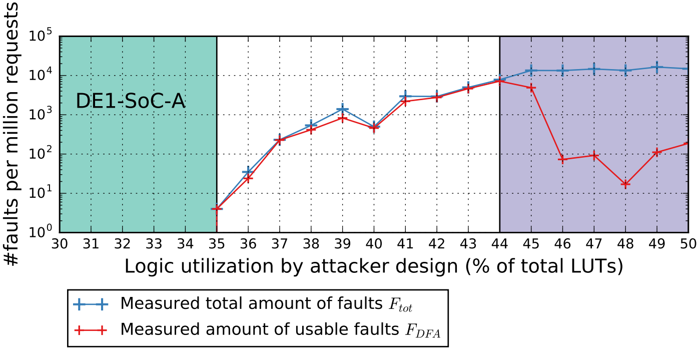

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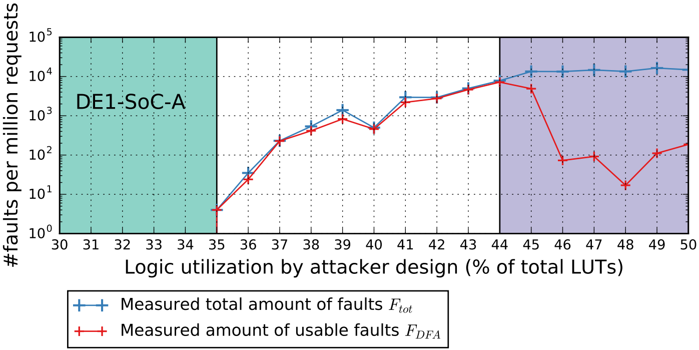

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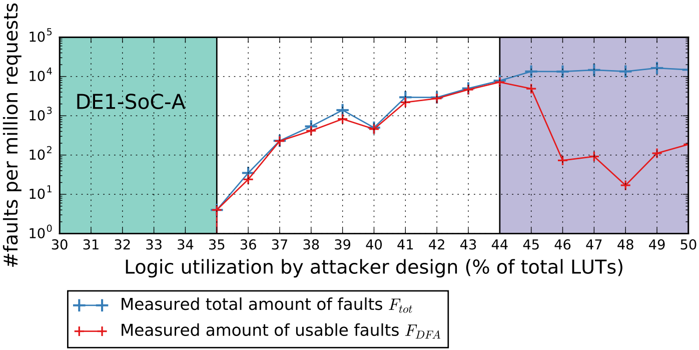

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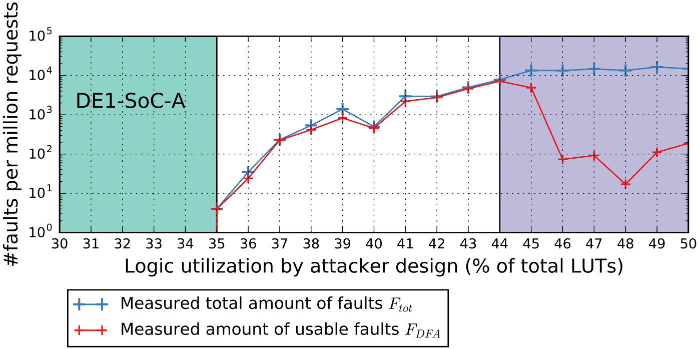

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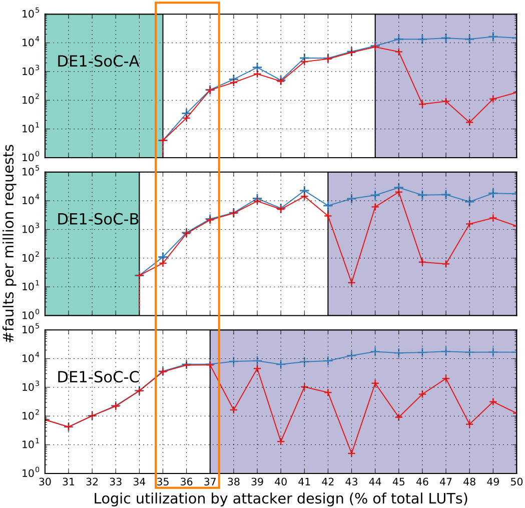

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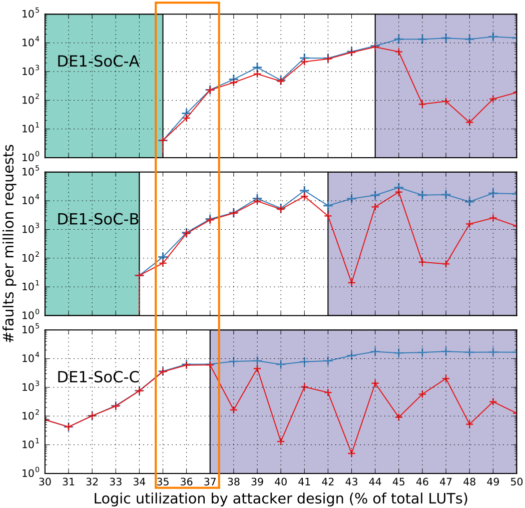
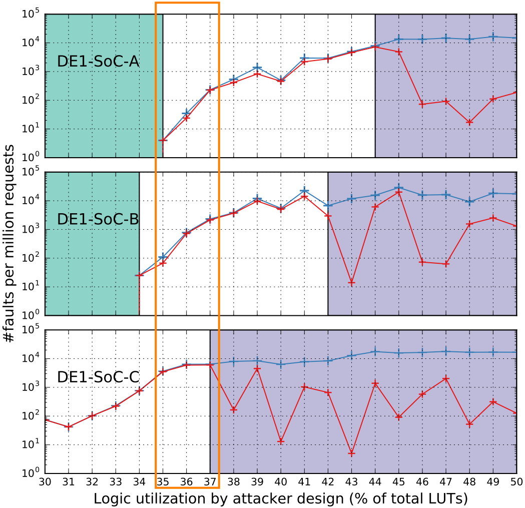


- Extended experiments: 3 different boards
- All boards vulnerable, Calibration finds params

J. Krautter, D.R.E. Gnad and M.B. Tahoori

Fault Injection Rate vs #RO



- Extended experiments: 3 different boards
- All boards vulnerable, Calibration finds params
- Process variation ⇒ Different optimal #RO

FPGAhammer: Remote Voltage Fault Attacks on Shared FPGAs

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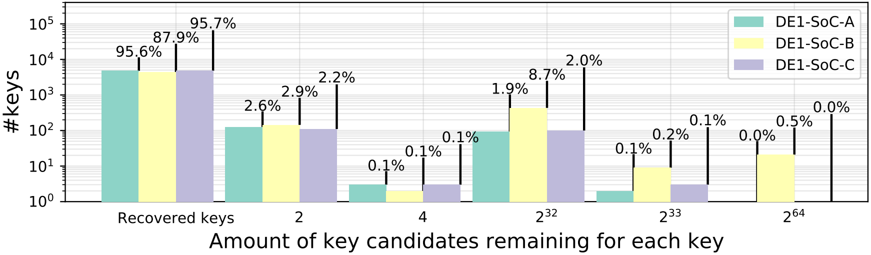
Key Recovery on 5000 random keys



- Experiments on DE1-SoC with best fault injection configuration

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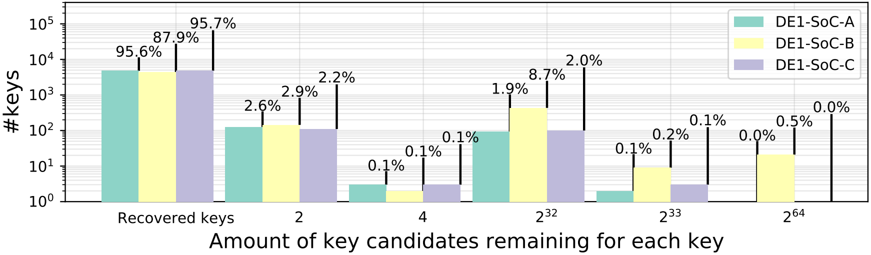

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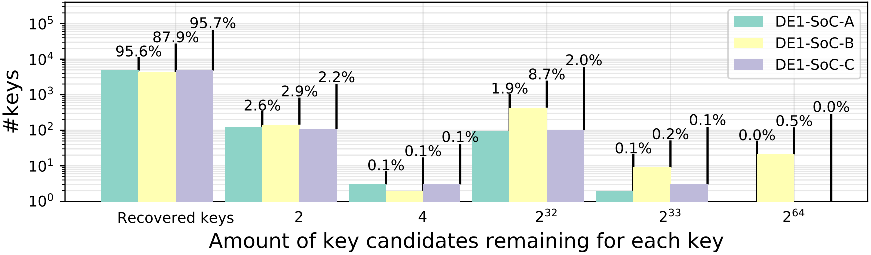

- Experiments on DE1-SoC with best fault injection configuration
- Majority of 5000 keys can be recovered
- Unrecovered keys due to **multi-byte faults**

Outline

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1. Background
2. Fault Injection and Analysis
3. Experimental Setup
4. Results
5. Discussion and Future Work
6. Conclusion

Discussion and Future Work

- Attack on fully constrained design on DE1-SoC with $< 50\%$ resources

Discussion and Future Work

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- Possible **mitigation**:
  - Internal sensors
  - Bitstream checking
  - Voltage islands

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- Logical isolation is not enough to prevent manipulation
- Threat model must be considered for FPGA multi-user environments
- Mitigation may require new/modified hardware

Thank you for your attention!

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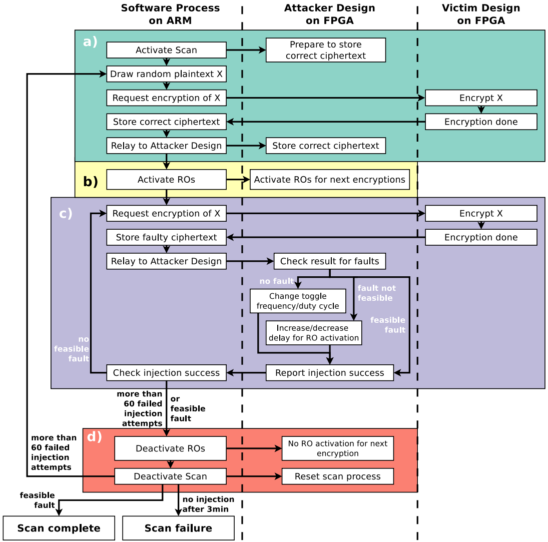
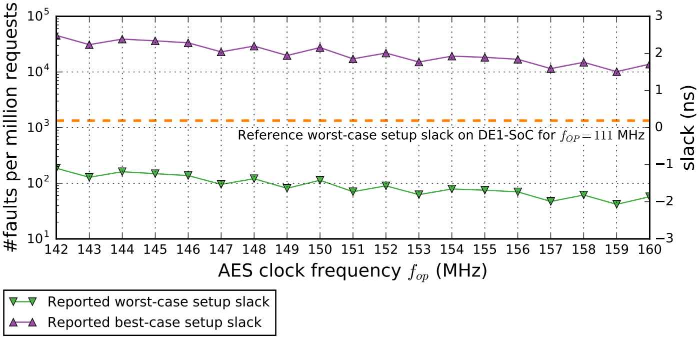
Additional Slides – Complete Scan Flow



Additional Slides – Slack Dependent Analysis



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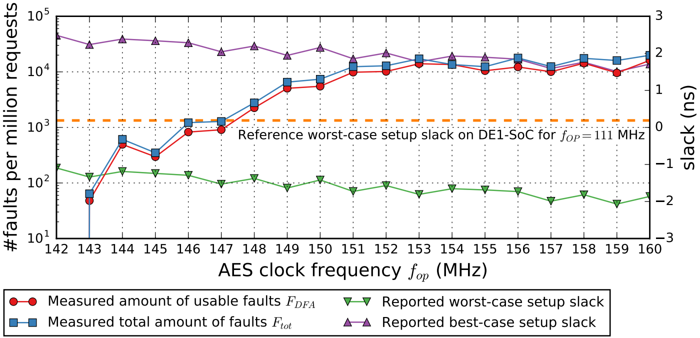
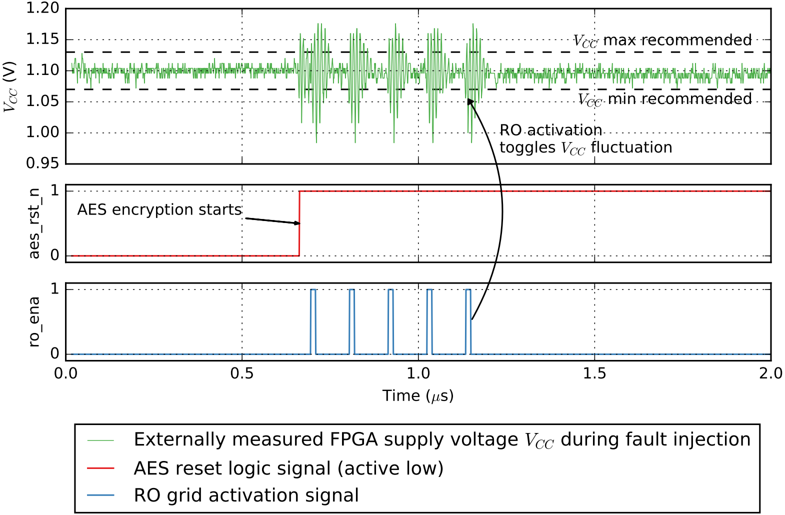


Additional Slides – Injection Process



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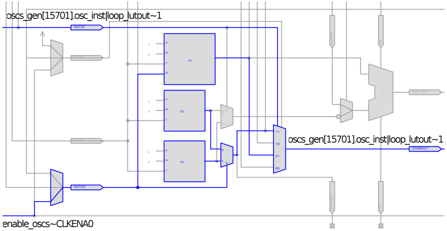
Additional Slides – RO Floorplan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oscs_gen[15701].osc_inst|loop_lutout~1
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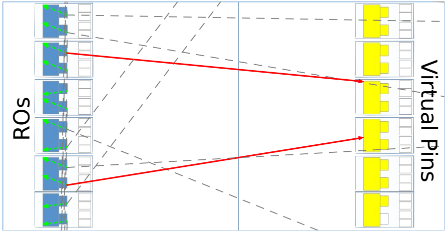
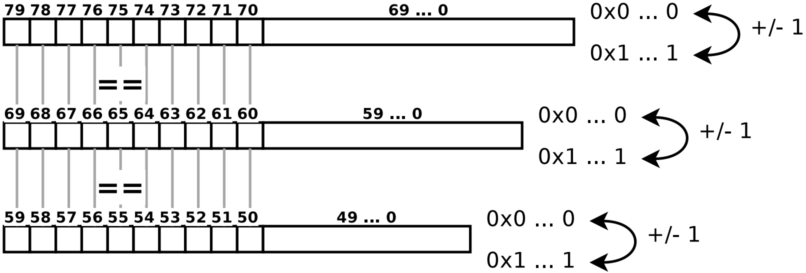


Additional Slides – Adder Test Design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0x0 ... 0
0x1 ... 1
+/- 1
==
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59 ... 0
0x0 ... 0
0x1 ... 1
+/- 1
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59 58 57 56 55 54 53 52 51 50
49 ... 0
0x0 ... 0
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